Half-Duplex *i*Coupler® Isolated RS-485 Transceiver

Preliminary Technical Data

ADM2483

FEATURES

RS-485 transceiver with electrical data isolation
Complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482:1987(E)
500kbps data rate
Slew rate limited driver outputs
Low power operation:
2.5mA max
Suitable for 5 V or 3 V operation (V_{DD1})
High common mode transient immunity: >25kV/µs
True failsafe receiver inputs
Glitch-free power-up/down protection
Thermal shutdown protection
Safety and regulatory approvals
UL recognition: 2500 V_{RMS} for 1 minute per UL 1577 (pending)
CSA Component Acceptance Notice #5A
VDE Certificate of Conformity
DIN EN 60747-5-2 (VDE 0884 Rev. 2):2003-01
DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000
V_{IORM} = 560V peak
Operating temperature range: -40° to 85°C
Wide body 16-lead SOIC package

APPLICATIONS

Low Power RS-485/RS-422 Networks
Isolated Interfaces
Building Control Networks
Multipoint Data Transmission Systems

GENERAL DESCRIPTION

The ADM2483 differential bus transceiver is an integrated, galvanically isolated component designed for bi-directional data communication on multi-point bus transmission lines. It is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A and ISO 8482:1987(E). The ADM2483 employs Analog Devices' *i*Coupler® technology to combine a 3-channel isolator, a 3-state differential line driver and a differential input receiver into a single package. The logic side of the device can be powered with either a 5V or a 3V supply while the bus-side is powered with a 5V supply.

FUNCTIONAL BLOCK DIAGRAM

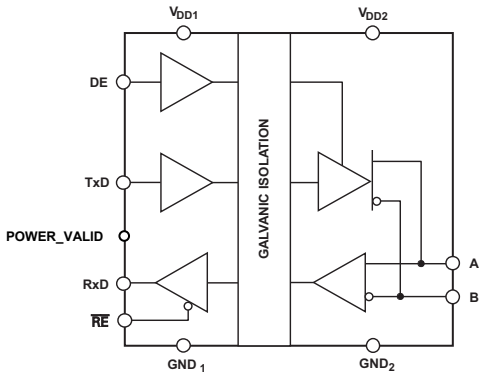


Figure 1.

The ADM2483 is slew limited to reduce reflections with improperly terminated transmission lines. The controlled slew rate limits the data rate to 500kbps. The input impedance of the ADM2483 is 96 kΩ allowing up to 256 transceivers on the bus. The ADM2483 driver has an active-high enable. The driver differential outputs and the receiver differential inputs are connected internally to form a differential I/O port that imposes minimal loading on the bus when the driver is disabled or when V_{DD1} or V_{DD2} =0. Also provided is an active-high receive disable which causes the receive output to enter a high impedance state.

The receiver inputs have a true failsafe feature which ensures a logic high output level when the inputs are open or shorted. This guarantees that the receiver outputs are in a known state before communication begins and when communication ceases.

The ADM2483 has current limiting and thermal shutdown features to protect against output short circuits and bus contention situations where these might cause excessive power dissipation.

Rev. PrC

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

SPECIFICATIONS

Table 1. 2.7 ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, T_A= T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Outputs:					
Differential Output Voltage, V_{OD}			5	V	R=∞, Test Circuit 1
	2.0		5	V	R=50Ω (RS-422), Test Circuit 1
	1.5		5	V	R=27Ω (RS-485), Test Circuit 1
	1.5		5	V	V_{TST}=-7V to 12V, V_{DD1}≥4.75, Test Circuit 2
Δ |V_{OD}| for Complementary Output States			0.2	V	R=27Ω or 50Ω, Test Circuit 1
Common Mode Output Voltage, V_{OC}			3	V	R=27Ω or 50Ω, Test Circuit 1
Δ |V_{OC}| for Complementary Output States			0.2	V	R=27Ω or 50Ω, Test Circuit 1
Output Short Circuit Current, V_{OUT}=High	-250		+250	mA	-7V≤V_{OUT}≤+12V
Output Short Circuit Current, V_{OUT}=Low	-250		+250	mA	-7V≤V_{OUT}≤+12V
Logic Inputs:					
Input High Voltage	0.7V_{DD1}			V	TxD, DE, $\overline{RE}$, PV
Input Low Voltage			0.25V_{DD1}	V	TxD, DE, $\overline{RE}$, PV
CMOS Logic Input Current (TxD, DE, $\overline{RE}$, PV)	-10	0.01	10	µA	TxD, DE, $\overline{RE}$, PV =V_{DD1} or 0V
RECEIVER					
Differential Inputs:					
Differential Input Threshold Voltage, V_{TH}	-200	-125	-30	mV	-7V≤V_{CM}≤+12V
Input Hysteresis		20		mV	-7V≤V_{CM}≤+12V
Input Resistance (A, B)	96	150		kΩ	-7V≤V_{CM}≤+12V
Input Current (A, B)			0.125	mA	V_{IN} =+12V
			-0.1	mA	V_{IN}=-7V
RxD Logic Output:					
Output High Voltage	V_{DD1}-0.1			V	I_{OUT}=20µA, V_A-V_B=0.2V
	V_{DD1}-0.4	V_{DD1}-0.2		V	I_{OUT}=4mA, V_A-V_B=0.2V
Output Low Voltage			0.1	V	I_{OUT}=-20µA, V_A-V_B=-0.2V
			0.4	V	I_{OUT}=-4mA, V_A-V_B=-0.2V
Output Short Circuit Current	7		85	mA	V_{OUT}=GND or V_{CC}
Three-State Output Leakage Current			±1	µA	-7V≤V_{OUT}≤+12V
POWER SUPPLY CURRENT					
Logic Side			2.5	mA	4.5V≤V_{DD1}≤5.5V, Outputs Unloaded, $\overline{RE}$=0V
			1.3	mA	2.7V≤V_{DD1}≤3.3V, Outputs Unloaded, $\overline{RE}$=0V
Bus Side			2.0	mA	Outputs Unloaded, DE=5V
			1.7	mA	Outputs Unloaded, DE=0V
COMMON MODE TRANSIENT IMMUNITY[1]	25			kV/µs	TxD=V_{DD1} or 0V, V_{CM}=1kV, Transient Magnitude=800V

[1] CM is the maximum common mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

TIMING SPECIFICATIONS

Table 2. 2.7 ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, T_A= T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Maximum Data Rate	500			kbps	
Propagation Delay t_{PLH}, t_{PHL}	250		620	ns	R_{LDIFF}=54Ω, C_{L1}= C_{L2}=100pF, Test Circuit 3
Skew t_{SKEW}			40	ns	R_{LDIFF}=54Ω, C_{L1}= C_{L2}=100pF, Test Circuit 3
Rise/Fall Time t_R, t_F	200		600	ns	R_{LDIFF}=54Ω, C_{L1}= C_{L2}=100pF, Test Circuit 3
Enable Time			1050	ns	R_L=500Ω, C_L =100pF, Test Circuit 4
Disable Time			1050	ns	R_L=500Ω, C_L =15pF, Test Circuit 4
Enable Time from Shutdown		5000		ns	R_L=500Ω, C_L =100pF, Test Circuit 4
RECEIVER					
Propagation Delay t_{PLH}, t_{PHL}	400		1050	ns	C_L=15pF, Test Circuit 5
Differential Skew t_{SKEW}			250	ns	C_L=15pF, Test Circuit 5
Enable Time		25	70	ns	R_L=1kΩ, C_L=15pF, Test Circuit 6
Disable Time		40	70	ns	R_L=1kΩ, C_L=15pF, Test Circuit 6
Enable Time from Shutdown		4000		ns	R_L=1kΩ, C_L=15pF, Test Circuit 6
Time to Shutdown	50	200	5000	ns	
POWER VALID INPUT					
Enable Time		1	2	µs	
Disable Time		3	5	µs	

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Parameter	Rating
V_{DD1}	-0.5V to +6V
V_{DD2}	-0.5V to +6V
Digital Input Voltage (RTS, $\overline{RE}$, TxD)	-0.5V to V_{DD1}+0.5V
Digital Output Voltage	
RxD	-0.5V to V_{DD1}+0.5V
DE	-0.5V to V_{DD2}+0.5V
Driver Output/Receiver Input Voltage	-9V to +14V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +150°C
Average Output Current per Pin	-35mA to +35mA
θ_{JA} Thermal Impedance	73°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapour Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω•	
Capacitance (Input-Output)[1]	C_{I-O}		3		pF	f = 1MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	

[1] Device considered a two-terminal device: pins 1, 2, 3,4,5,6,7, and 8 shorted together and pins 9,10,11,12,13,14,15, and 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADM2483 will be approved by the following organizations upon product release:

Table 5.

UL[3]	CSA	VDE[4]
To be recognized under 1577 component recognition program	Approved under CSA Component Acceptance Notice #5A	Approved according to: DIN EN 60747-5-2 (VDE 0884 Rev. 2):2002-04 DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000

[3] In accordance with UL1577, each ADM2483 is proof tested by applying an insulation test voltage ≥3000 Vrms for 1 second (current leakage detection limit = 5 μA)
[4] In accordance with VDE 0884, each ADM2483 is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V_{RMS}	1-minute duration.
Minimum External Air Gap (Clearance)	L(I01)	7.40 min.	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.51 min.	mm	Measured from input terminals to output terminals, shortest distance path along body.
.				
Minimum Internal Gap (Internal Clearance)		0.02 min.	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110,1/89,Table 1)

VDE 0884 INSULATION CHARACTERISTICS

Table 7.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, for rated mains voltage			
≤ 150 Vrms		I to IV	
≤ 300 Vrms		I to III	
≤ 400 Vrms		I to II	
Climatic classification		40/85/21	
Pollution degree (DIN VDE 0110, Table 1)		2	
Maximum working insulation voltage	V_{IORM}	400	V_{PEAK}
Input to output test voltage, Method b1	V_{PR}	1050	V_{PEAK}
$V_{IORM} \times 1.875 = V_{PR}$, 100% production test,			
t_m = 1sec, partial discharge < 5 pC			
Input to output test voltage, Method a			
(After environmental tests Subgroup 1)			
V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC		896	Vpeak
(After input and/or safety test Subgroup 2/3)			
V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	Vpeak
Highest allowable over-voltage			
(Transient over-voltage, t_{TR} =10 sec)	V_{TR}	4000	V_{PEAK}
Safety-limiting values (maximum value allowed in the event of a failure. See thermal derating curve, Figure 1)			
Case temperature	TS		°C
Input current	$I_{S, INPUT}$		mA
Output current	$I_{S,OUTPUT}$		mA
Insulation resistance at Ts, V_{IO} = 500 V	Rs	$>10^9$	Ω

This isolator is suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

"*" marking on packages denotes VDE 0884 approval for 560 V peak working voltage.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

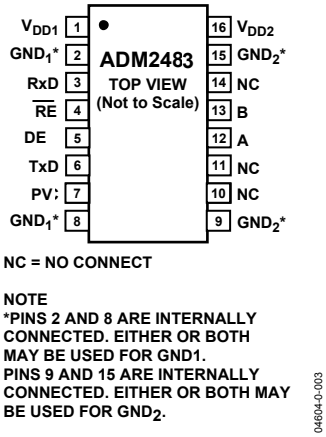
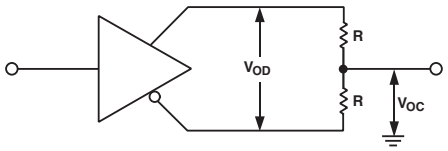


Figure 2.

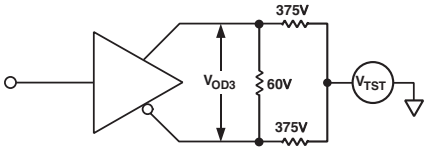
Table 8.

Pin	Mnemonic	Function
1	V_{DD1}	Power supply, logic side.
2, 8	GND_1	Ground, logic side.
3	R×D	Receiver output.
4	$\overline{RE}$	Receiver enable.
5	DE	Driver Enable
6	TxD	Transmit data.
7	PV	Power Valid. Used during power-up/down. See applications information.
9, 15	GND_2	Ground, bus side.
10, 14	NC	No Connect.
12	A	Noninverting driver output/receiver input.
13	B	Inverting driver output/receiver input.
16	V_{DD2}	Power supply, bus side.

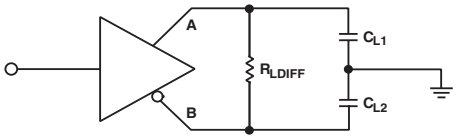
TEST CIRCUITS



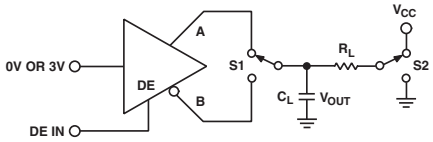
Test Circuit 1. Driver Voltage Measurement



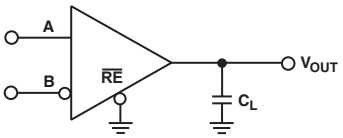
Test Circuit 2. Driver Voltage Measurement



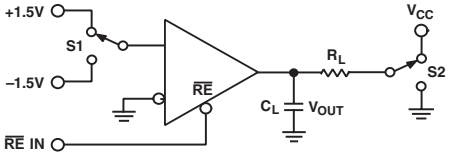
Test Circuit 3. Driver Propagation Delay



Test Circuit 4. Driver Enable/Disable



Test Circuit 5. Receiver Propagation Delay



Test Circuit 6. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

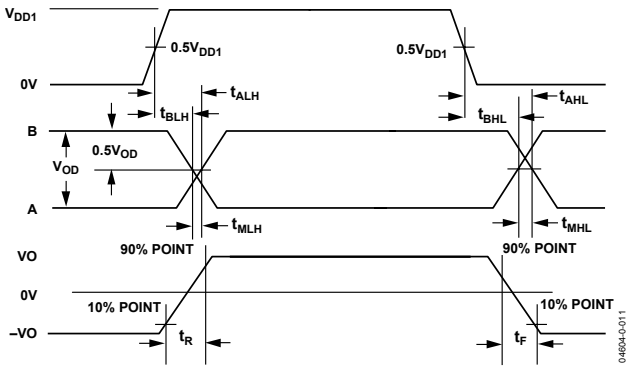


Figure 3. Driver Propagation Delay, Rise/Fall Timing

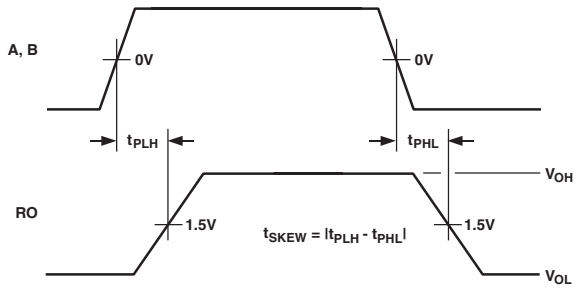


Figure 4. Receiver Propagation Delay

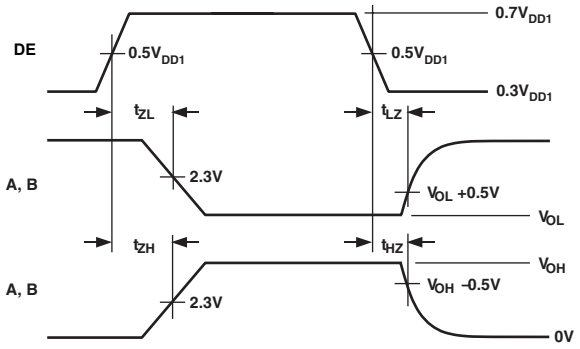


Figure 5. Driver Enable/Disable Timing

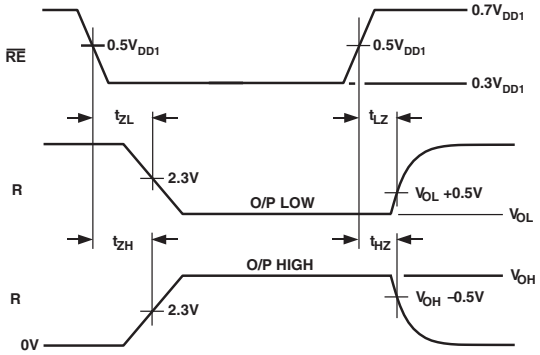


Figure 6. Receiver Enable/Disable Timing

TYPICAL PERFORMANCE CHARACTERISTICS

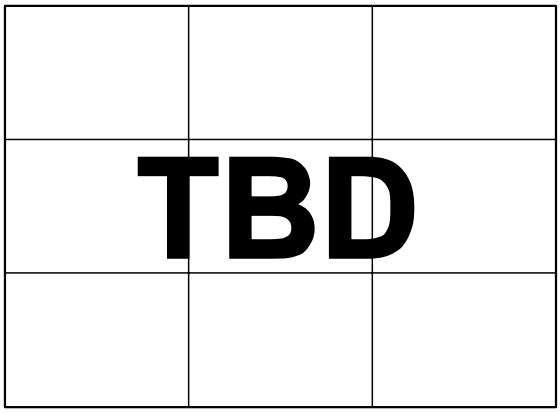


Figure 7. Unloaded Supply Current vs. Temperature

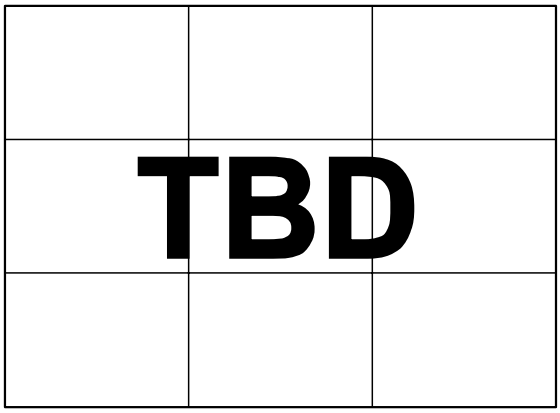


Figure 10. Receiver Output Low Voltage vs. Temperature

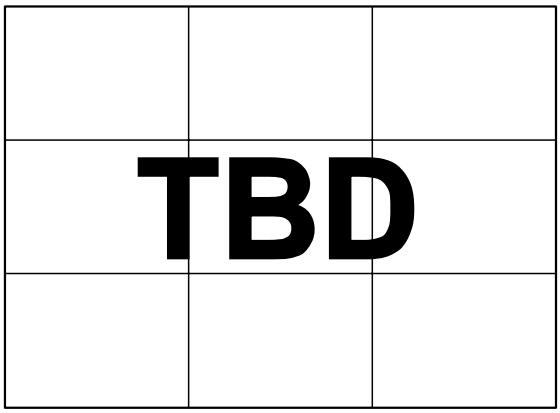


Figure 8. Output Current vs. Receiver Output Low Voltage

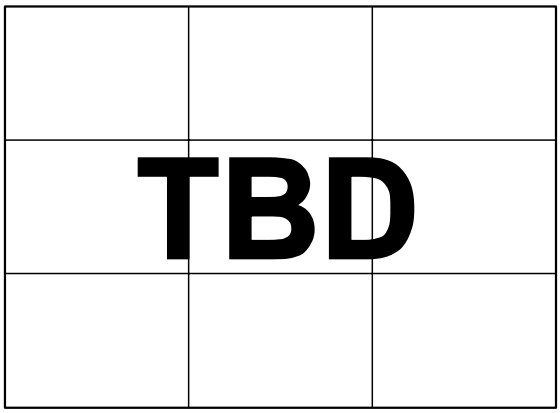


Figure 11. Receiver Output High Voltage vs. Temperature

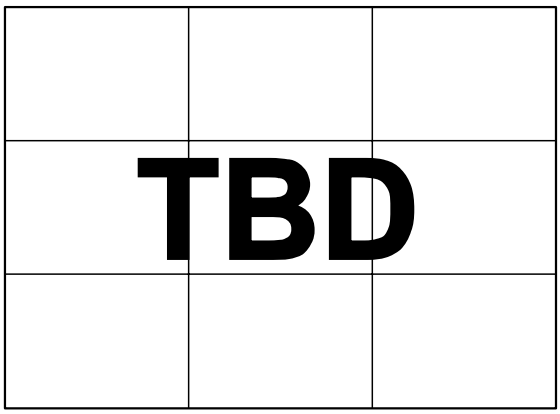


Figure 9. Output Current vs. Receiver Output High Voltage

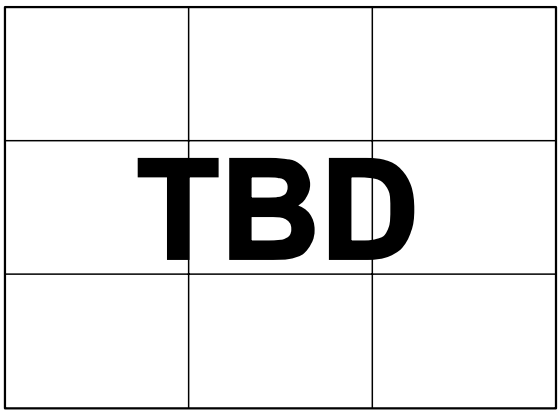


Figure 12. Driver Output Current vs. Differential Output Voltage

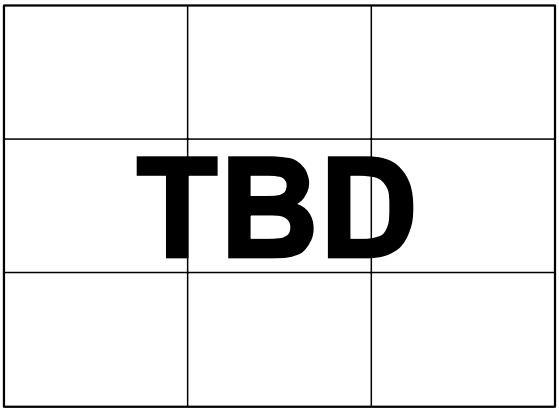


Figure 13. Output Current vs. Driver Output Low Voltage

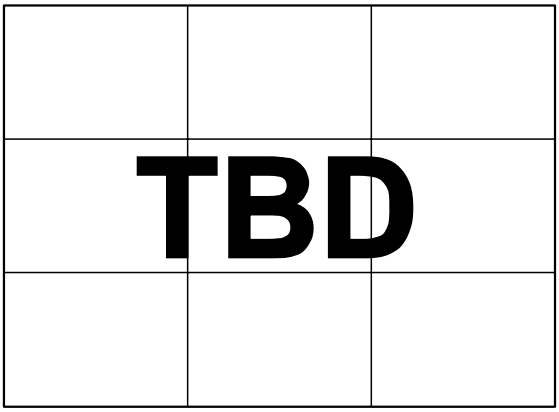


Figure 16. Receiver Propagation Delay vs. Temperature

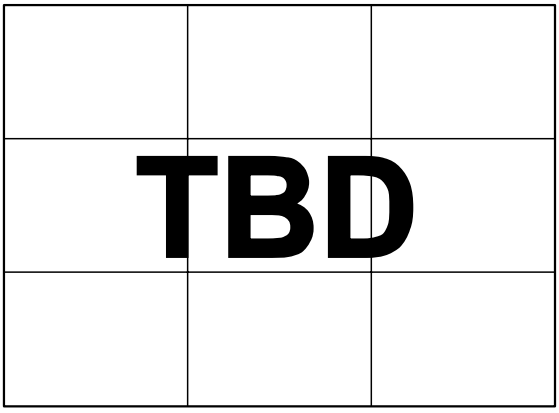


Figure 14. Output Current vs. Driver Output High Voltage

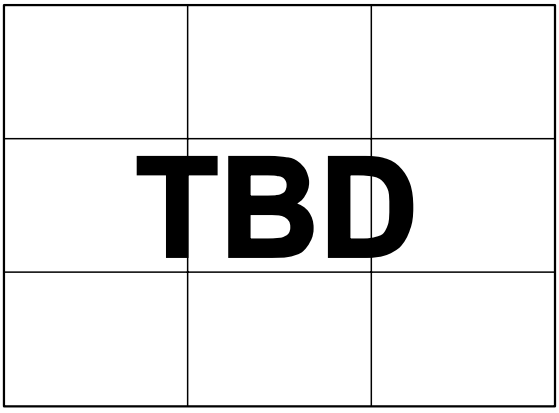


Figure 17. Driver/Receiver Propagation Delay (115kbps)

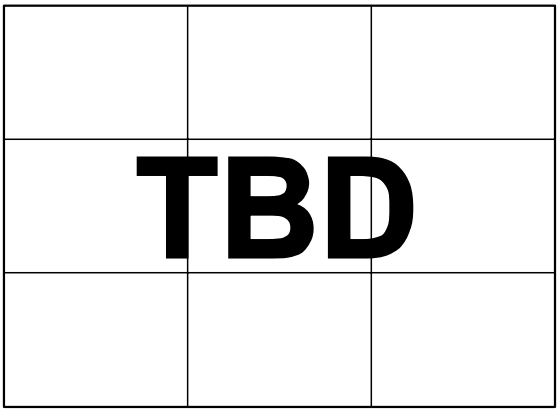


Figure 15. Driver Propagation Delay vs. Temperature

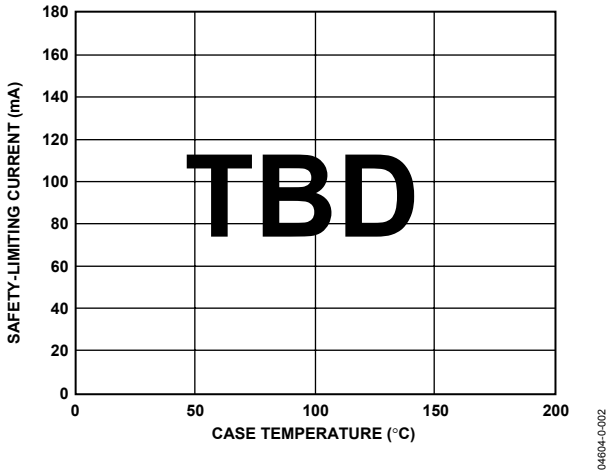


Figure 18 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2483, electrical isolation is implemented on the logic side of the interface. Therefore the part has two main sections; a digital isolation section and a transceiver section (see figure 19). Driver input and data enable signals, applied to the TxD and DE pins respectively and referenced to logic ground (GND_1), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

iCoupler® Technology

The digital signals are transmitted across the isolation barrier using *i*Coupler® technology. This technique uses chip-scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms which are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

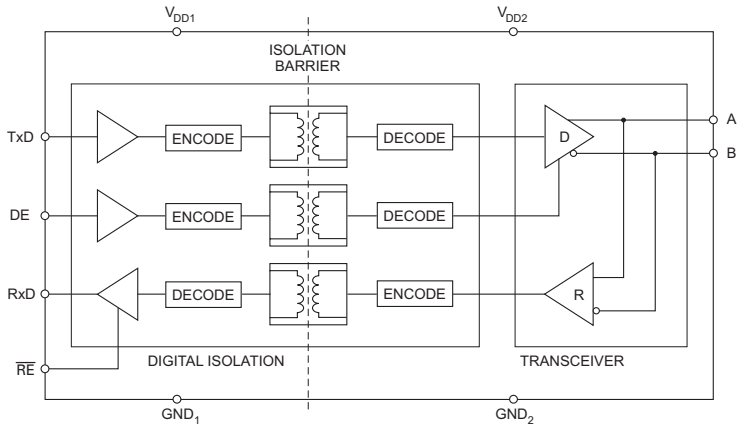


Figure 19. ADM2483 Digital Isolation and Transceiver Sections

TRUTH TABLES

The following truth tables use these abbreviations:

Letter	Description
H	High level
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 9.Transmitting

SUPPLY STATUS		INPUTS		OUTPUTS	
V_{DD1}	V_{DD2}	DE	T×D	A	B
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	X	X	Z	Z
Off	Off	X	X	Z	Z

Table 10. Receiving

SUPPLY STATUS		INPUTS		OUTPUT
V_{DD1}	V_{DD2}	A-B (V)	$\overline{RE}$	R×D
On	On	>-0.03	L or NC	H
On	On	<-0.2	L or NC	L
On	On	-0.2 <A-B<-0.03	L or NC	Indeterminate
On	On	Inputs Open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	On	X	L or NC	H
Off	Off	X	L or NC	L

POWER-UP/POWER-DOWN CHARACTERISTICS

The power-up/power-down characteristics of the ADM2483 are in accordance with the supply thresholds shown in table 11. Upon power-up, the ADM2483 output signals (A, B and RxD) reach their correct state once both supplies have exceeded their thresholds. Upon power-down, the ADM2483 output signals retain their correct state until at least one of the supplies drops below its power down threshold. When the V_{DD1} power-down threshold is crossed, the ADM2483 output signals reach their unpowered states within 4 µs.

Table 11. Power Up/Power-Down Thresholds

Supply	Transition	Threshold (V)
V_{DD1}	Power Up	2.0
V_{DD1}	Power Down	1.0
V_{DD2}	Power Up	3.3
V_{DD2}	Power Down	2.4

Figure 21. V_{DD2} Power Up/Down

THERMAL SHUTDOWN

The ADM2483 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER FAIL-SAFE INPUTS

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating or short-circuited.

MAGNETIC FIELD IMMUNITY

The ADM2483 is immune to external magnetic fields. The ADM2483's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The analysis below defines the conditions under which this may occur. The ADM2483's 3V operating condition is examined as it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0V in amplitude. The decoder has sensing thresholds at about 0.5V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The induced voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum\prod r_n^2 \; ; \; n = 1,2,\ldots,N$$

where:
β = magnetic flux density (Gauss)
N = number of turns in receiving coil
r_n = radius of nth turn in receiving coil (cm)

Given the geometry of the receiving coil and an imposed requirement that the induced voltage be at most 50% of the 0.5V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 22.

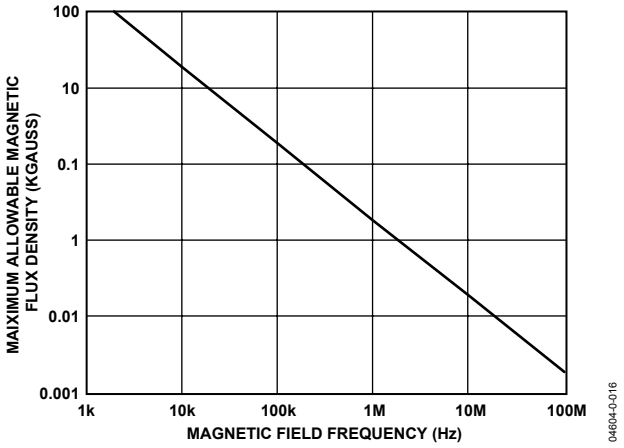


Figure 22. Maximum Allowable External Magnetic Flux Density.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 KGauss induces a voltage of 0.25V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and was of the worst-case polarity) it would reduce the received pulse from > 1.0V to 0.75V—still well above the 0.5V sensing threshold of the decoder.

As a convenience to the user, the above magnetic flux density values are shown below in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2483 transformers.

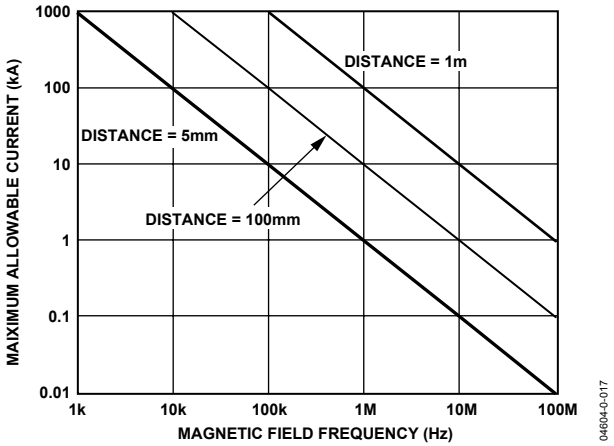


Figure 23. Maximum Allowable Current for Various Current-to-ADM2483 Spacings.

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

POWER_VALID INPUT

To avoid glitches on outputs 'A' and 'B' caused by slow power-up and power-down transients on V_{DD1} (>100µs/V), the ADM2483 features a power_valid (PV) digital input. This pin should be driven low until V_{DD1} exceeds 2.0V. When V_{DD1} is greater than 2.0V, this pin should be driven high. Conversely, on power down, PV should be driven low before V_{DD1} reaches 2.0V.

The power_valid input can be driven, for example, by the output of a system reset circuit such as the ADM809Z, which has a threshold voltage of 2.32V.

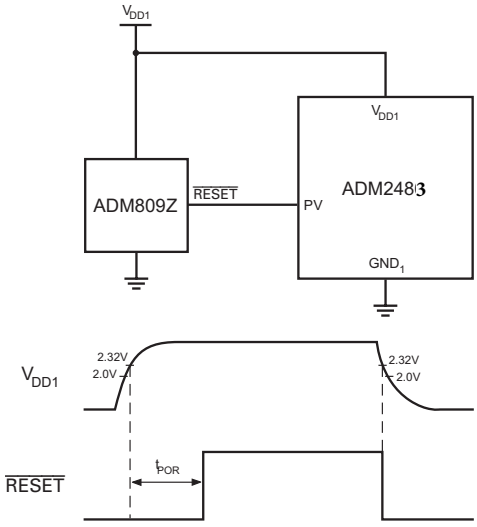


Figure 24. Driving PV with ADM809Z

ISOLATED POWER SUPPLY CIRCUIT

The ADM2483 requires isolated power capable of 5V at 100mA to be supplied between V_{DD2} and GND_2 pins. If no suitable integrated power supply is available, then a discrete circuit such as the one in figure 25 can be used. A center tapped transformer provides electrical isolation. The primary winding is excited with a pair of square waveforms which are 180° out of phase with each other. A pair of schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated power supply to the ADM2483's bus-side circuitry.

To create the pair of square waves, a D-type flip-flop with complementary Q/$\overline{Q}$ outputs is used. The flip-flop can be connected so that output Q follows the clock input signal. If no local clock signal is available, then a simple digital oscillator can be implemented with a hex inverting schmitt trigger and resistor and capacitor. In this case, values of 3.9kΩ and 1nF generate a 364kHz square wave. A pair of discrete NMOS transistors, being switched by the Q/$\overline{Q}$ flip-flop outputs, conduct current through the center tap of the primary transformer winding in an alternating fashion.

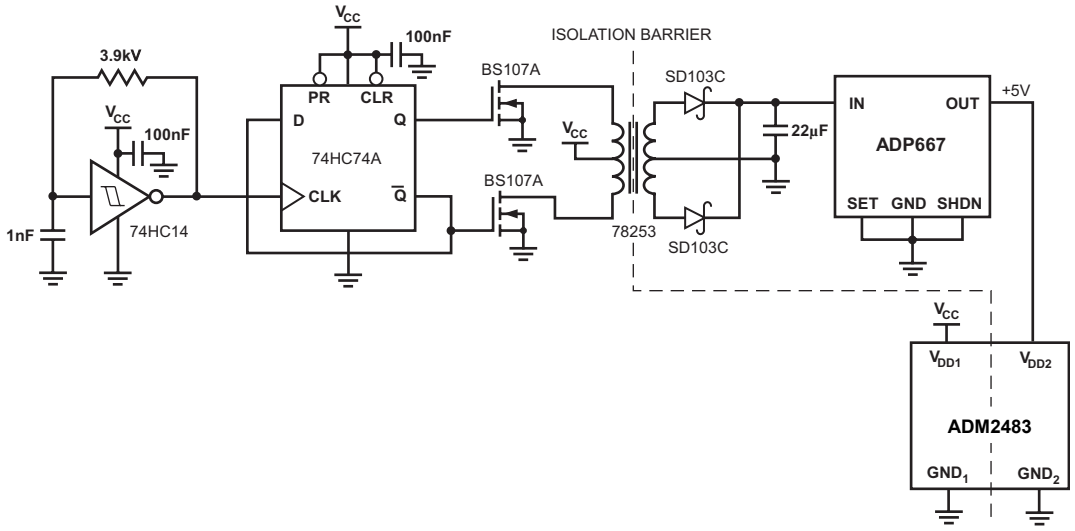


Figure 25. Isolated Power Supply Circuit

OUTLINE DIMENSIONS

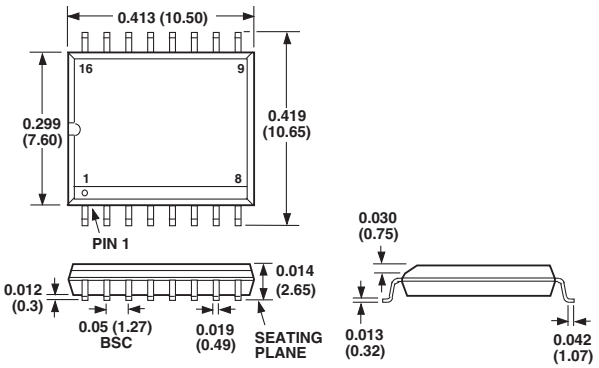


Figure 26. 16-Lead Wide-Body Small Outline Package [SOIC]

(RW-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Data Rate (kbps)	Temperature Range	Package Description	Package Option
ADM2483BRW	500	−40°C to +85°C	16-Lead Wide Body SOIC	RW-16

The addition of an "-RL" suffix designates a 13" (1000 units) tape and reel option.

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PR04736-0-6/04(PrC)